**Lab Assignment 2: Main Memories**

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**Part A: DRAM Traces [50 pts]**

Write a C/C++ program that takes as input the following parameters:

-w [address\_width] -m [address\_mapping] -n [num\_requests] -p [address\_pattern] -t [type\_pattern]

And generate a DRAM trace with the specified patterns. The trace should look like Address:type, where address is in hex and type is either R (for read) or W (for write).

For example:

0x12345680 R

0x4cbd56c0 W

0x35d46f00 R

0x696fed40 W

0x7876af80 R

* DRAM Architecture: you have to match the structure of the “DDR3\_2Gb\_x8” in the MCsim simulator to be able to also use your traces for PartB. Figure out the number of ranks, channels, banks, ..etc for this structure from MCsim.
* Your program should be able to generate the following address and type patterns:
  + Address patterns:
    - Sequential
    - Random
    - All row hit
    - All row conflicts
  + Type patterns:
    - All R
    - All W
    - Switching: R, W, R, W,..etc.
* You should also consider the following mappings (where RW: Row, RNK: Rank, BNK: Bank,CL: Column):
  + RW-RNK-BNK-CL
  + RW-CL-RNK-BNK
  + RNK-BNK-CL-RW

**Answer:**

DRAM\_Traces.cpp (C++ code file) and dram\_traces.txt (output trace file) attached. The output trace file is slightly different to match the MCsim format: instead of 0x12345680 R , instead it stores like this 0x12345680 Read 0, to match the MCsim format

Command to compile the C++ file:

g++ DRAM\_Traces.cpp -o < filename >

Command to run the C++ file:

./< filename> -w [address\_width] -m [address\_mapping] -n [num\_requests] -p [address\_pattern] -t [type\_pattern]

Number of bits for Banks: 3

Number of bits for Rows: 15

Number of bits for Columns: 10

Number of bits for Offset bits: 6

* For address pattern use (all lower case):
  + sequential
  + random
  + row-hit
  + row-conflict
* For type patterns use:
  + R for read
  + W for write
  + Switching:
    - RW or anything else than the above
* For Address Mapping use:
  + row-bnk-col
  + row-col-bnk
  + bnk-col-row

Example of commands to run:  
g++ DRAM\_Traces.cpp -o DRAM\_Traces

./ DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "sequential" -t "R"

Simulation output of the example: dram\_traces.txt output of the example:

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**Part B: Simulating Off-chip Memory [50 pts]**

1. **[10 pts] Use your tool from Part A to generate the following traces, where each trace should have 10K requests and the address mapping should be row:bank:column (assume a single channel and single rank).**

* **All Read, Sequential Trace**
* **All Read, Random Trace**
* **All Read, Conflict Trace**
* **All Read, Hit Trace**
* **Switching, Hit Trace**

**Answer:**

* All Read, Sequential Trace

Command: ./DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "sequential" -t "R"

Output file: seq\_NG.txt

* All Read, Random Trace

Command: ./DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "random" -t "R"

Output file: rand\_NG.txt

* All Read, Conflict Trace

Command: ./DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "row-conflict" -t "R"

Output file: row\_conf\_NG.txt

* All Read, Hit Trace

Command: ./DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "row-hit" -t "R"

Output file: row\_hit\_NG.txt

* Switching, Hit Trace

Command: ./DRAM\_Traces -w 28 -m "row-bnk-col" -n 10000 -p "row-hit" -t "RW"

Output file: switch\_row\_hit\_NG.txt

1. **[10 pts] Familiarize yourself with MCsim simulator. Start with getting MCSim from here:** <https://github.com/uwuser/MCsim> **and read the README file.**
2. **[15 pts] Configure MCsim to use FR-FCFS and run all the 5 traces from step 1. Make sure that the address mapping in MCsim are set correctly. In MCsim the address mapping is determined in the ini file where each segment is coded as follows: Rank[0], BankGroup[1], Bank[2], SubArray[3], Row[4], Col[5]. So, AddressMapping=425 means row:bank:column.**

**Draw a graph that compares the execution time of all the five traces.**

**Answer:**

* Simulation output of All Read, Sequential Trace:

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* Simulation output of All Read, Random Trace

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* Simulation output of All Read, Conflict Trace

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* Simulation of All Read, Hit Trace

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* Simulation output of Switching, Hit Trace

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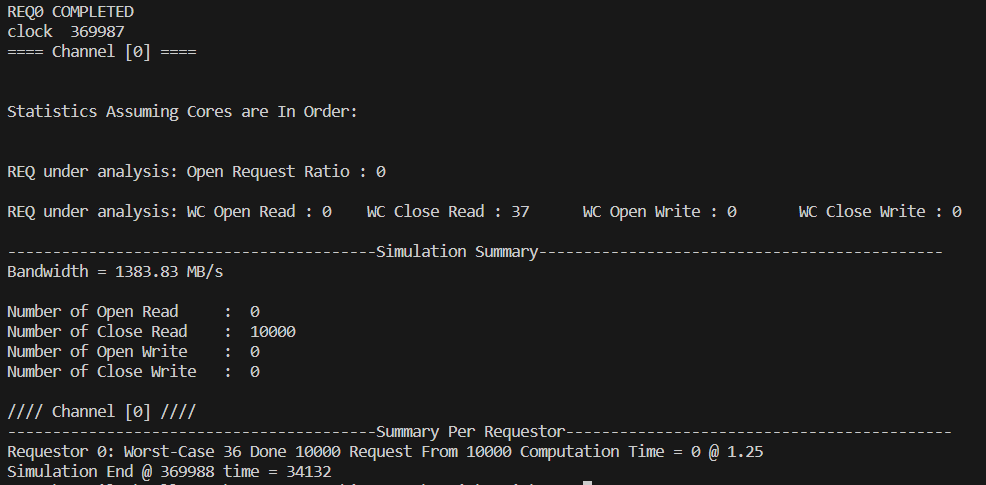
The execution time for cases: Time (10-3 seconds) = Clock Ticks / Clock frequency, For DDR3 with 1600H device speed clock frequency would be 800 MHz

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Address Mapping** | **Open Read** | **Close Read** | **Open Write** | **Close Write** | **Bandwidth (MB/s)** | **Cycles** | **Clock Ticks** | **Time (10-3 sec)** |
| All Read, Sequential Trace | 9375 | 625 | 0 | 0 | 3624.96 | 141244 | 19197 | 0.02399625 |
| All Read, Random Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 41061 | 0.05132625 |
| All Read, Conflict Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 57331 | 0.07166375 |
| All Read, Hit Trace | 9999 | 1 | 0 | 0 | 3938.13 | 130012 | 14597 | 0.01824625 |
| Switching, Hit Trace | 4999 | 1 | 5000 | 0 | 3303.1 | 155007 | 20058 | 0.0250725 |

1. **[10 pts] Change the FR-FCFS ini file to use close-page policy and repeat the experiments and redraw the graph similar to part 3.**

**Answer:**

* Simulation output of All Read, Sequential Trace:



* Simulation output of All Read, Random Trace

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* Simulation output of All Read, Conflict Trace

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* Simulation of All Read, Hit Trace

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* Simulation output of Switching, Hit Trace

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The execution time for cases: Time (10-3 seconds) = Clock Ticks / Clock frequency, For DDR3 with 1600H device speed clock frequency would be 800 MHz

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Address Mapping** | **Open Read** | **Close Read** | **Open Write** | **Close Write** | **Bandwidth (MB/s)** | **Cycles** | **Clock Ticks** | **Time (10-3 sec)** |
| All Read, Sequential Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 34132 | 0.42665 |
| All Read, Random Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 33149 | 0.4143625 |
| All Read, Conflict Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 47337 | 0.5917125 |
| All Read, Hit Trace | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 32175 | 0.4021875 |
| Switching, Hit Trace | 0 | 5000 | 0 | 5000 | 1383.83 | 369988 | 35254 | 0.440675 |

1. **[15 pts] Use the trace “All Read, Random Trace” to compare all the controller systems supported by MCsim. Plot the results in a bar-chart.**

**Answer:**

* Simulation output of FR-FCS (Policy: Open):

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* Simulation output of FR-FCFS (Policy: Close):

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* Simulation output of AMC:

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* Simulation output of BLISS:

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* Simulation output of DCMC:

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* Simulation output of FCFS:

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* Simulation output of FRFCS:

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* Simulation output of MAG:

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* Simulation output of MCMC:

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* Simulation output of MEDUSA:

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* Simulation output of ORP:

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* Simulation output of PAR-BS:

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* Simulation output of PIECAS:

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* Simulation output of PMC:

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* Simulation output of RankReOrder:

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* Simulation output of ReOrder:

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* Simulation output of ROC:

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* Simulation output of Round:

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* Simulation output of RTMem:

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The execution time for All Read, Random Trace with all controllers supported by MCsim are as follows, Time (10-3 seconds) = Clock Ticks / Clock frequency, For DDR3 with 1600H device speed clock frequency would be 800 MHz So, Time (10-3 seconds) for different traces would be:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Controller System** | **Open Read** | **Close Read** | **Open Write** | **Close Write** | **Bandwidth (MB/s)** | **Cycles** | **Clock Ticks** | **Time (10-3 sec)** |
| FR-FCFS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 47377 | 0.05922125 |
| AMC | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 34305 | 0.04288125 |
| BLISS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 34771 | 0.04346375 |
| DCMC | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 31503 | 0.03937875 |
| FCFS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 30982 | 0.0387275 |
| FRFCS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 30648 | 0.03831 |
| MAG | 0 | 10000 | 0 | 0 | 1765.55 | 289996 | 24682 | 0.0308525 |
| MCMC | 0 | 10000 | 0 | 0 | 1280.02 | 399994 | 32999 | 0.04124875 |
| MEDUSA | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 36326 | 0.0454075 |
| ORP | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 30850 | 0.0385625 |
| PAR-BS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 30656 | 0.03832 |
| PIECAS | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 31869 | 0.03983625 |
| PMC | 0 | 10000 | 0 | 0 | 1089.42 | 469978 | 39163 | 0.04895375 |
| RankReOrder | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 31678 | 0.0395975 |
| ReOrder | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 31568 | 0.03946 |
| ROC | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 30760 | 0.03845 |
| Round | 0 | 10000 | 0 | 0 | 1383.83 | 369988 | 53181 | 0.06647625 |
| RTMem | 0 | 10000 | 0 | 0 | 1219.1 | 419983 | 32425 | 0.04053125 |